UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,419	10/20/2003	Martin Perner	P2002,0892	2800

24131 7590 05/09/2005

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
NGUYEN, VINH P	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,419	PERNER, MARTIN	
	Examiner	Art Unit	
	VINH P. NGUYEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-12,20-25 and 29* is/are rejected.

7)☒ Claim(s) *2-7,13-19,26-28 and 30-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0504*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 25 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al (Pat # 6,446,164).

As to claims 25 and 29, Nguyen et al suggest that the semiconductor module (processor (101)) has 84 pins/contact terminals provided for external data interchanges, address interchanges and/or command interchange during normal operation (see column 6., lines 5-28). Among these terminals, there is a further contact terminal (RSVD (40)) used for testing purpose. It appears that the step of initializing and setting a mode of operation for ascertaining and outputting test information during normal operation of the semiconductor module (processor (101)) is performed through this further contact terminal (RSVD (40)).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1,8-12, 20-25 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Gillenwater et al (Pat # 5,546,406).

As to claims 1,12, Gillenwater et al disclose a semiconductor module (900) having a plurality of contact terminals (RST,TD1,TD0,TMS,...) for external data interchange, address interchange and/or command interchange, at least one further contact terminal (901-1or 901-2 or 901-3 or 901-4) used for testing but not used for external data interchange, address interchange and/or command interchange and a main circuit (ASIC Logic in combination with 903-1 or 903-2, or 903-3 or 903-4) connected to further contact terminal (901-1or 901-2 or 901-3 or 901-4).

As to claims 8-12 and 20-23 it appears that the output/BSRC/BIST (904-1 or 904-2 or 904-3 or 904-4) is a combination of both measurement circuit and output circuit electrically connected to the further contact terminal (902-1 or 902-2 or 902-3 or 902-4) for outputting the test data to the outside.

As to claim 24, the output/BSRC/BIST (904-1 or 904-2 or 904-3 or 904-4) outputs test data toward an outside through the further contact terminal (902-1 or 902-2 or 902-3 or 902-4).

As to claims 25 and 29, it appears that the step of initializing and setting a mode of operation for ascertaining and outputting test information during normal operation of the semiconductor module (900) is performed through this further contact terminal (901-1or 901-2 or 901-3 or 901-4).

5. Claims 2-7,15-19,26-28 and 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not disclose the first reception circuit coupled to the further contact terminal for receiving and decoding a function code sequence for setting the test sequence or the configuration sequence, a first shift register connected to the further contact terminal for serially receiving input code signal sequence, a first register circuit for storing a digitally coded input code, a first comparison circuit connected to the first shift register and first register circuit, a first enable circuit connected to the further contact terminal ,a second shift register, a second register circuit, a second embale circuit, a third shift register, a control unit , a measurement unit, a configuration register.

6. Claims 13-14 are objected to because of the following informalities:

In claim 13, it is unclear what "configuration settings" are and where are they from.

In claim 14, should this claim depend from claim 13 instead of claim 12 because "configuration register" has not been recited in claim 12.. Appropriate correction is required.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Revilla et al (pat # 5,553;236) disclose mehd and apparatus for testing a clock stopping/starting function of a low power mode in a data processor.

Hapke (pat # 4,336,495) disclose integrated circuit arrangement in MOS technology with filed effect transistors.

Stambaugh et al (pat # 4,970,454) disclose packaged semiconductor device with test circuits for determining fabrication parameters.

Lysinger (pa # 5,982,188) disclose testmode control circuit of an integrated circuit device.

Bourekas et al (pat # 5,317,711) disclose structure and method for monitoring an internal cache.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VINH P NGUYEN
Primary Examiner
Art Unit 2829
04/28/05